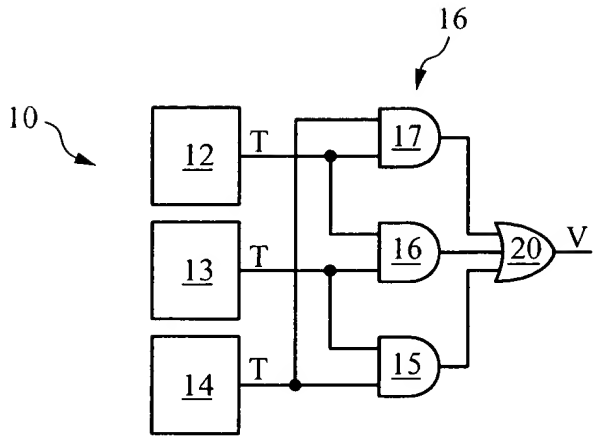


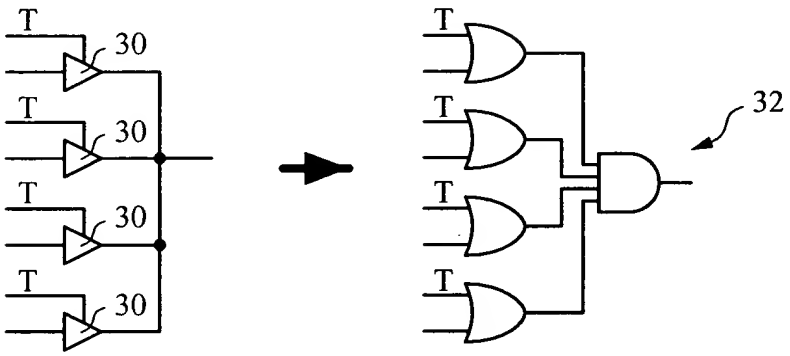
Triple Redundancy with Voting

FIG. 1

SEU Mitigation Truth Table

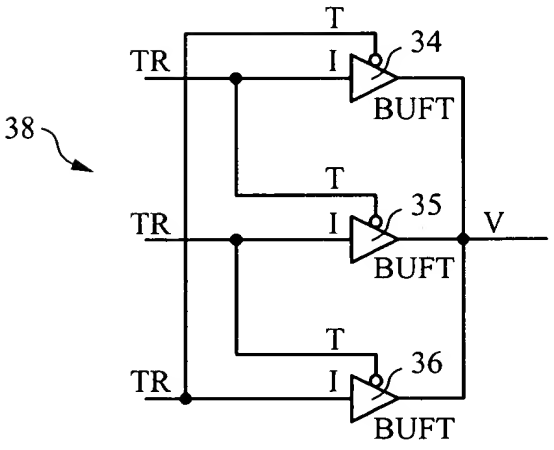
TR0	TR1	TR2	V
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

FIG. 2



Virtex BUFT Structure

FIG. 3



Voting circuit with BUFTs

FIG. 4

TRV Truth Table

TR0	TR1	TR2	V
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

FIG. 5

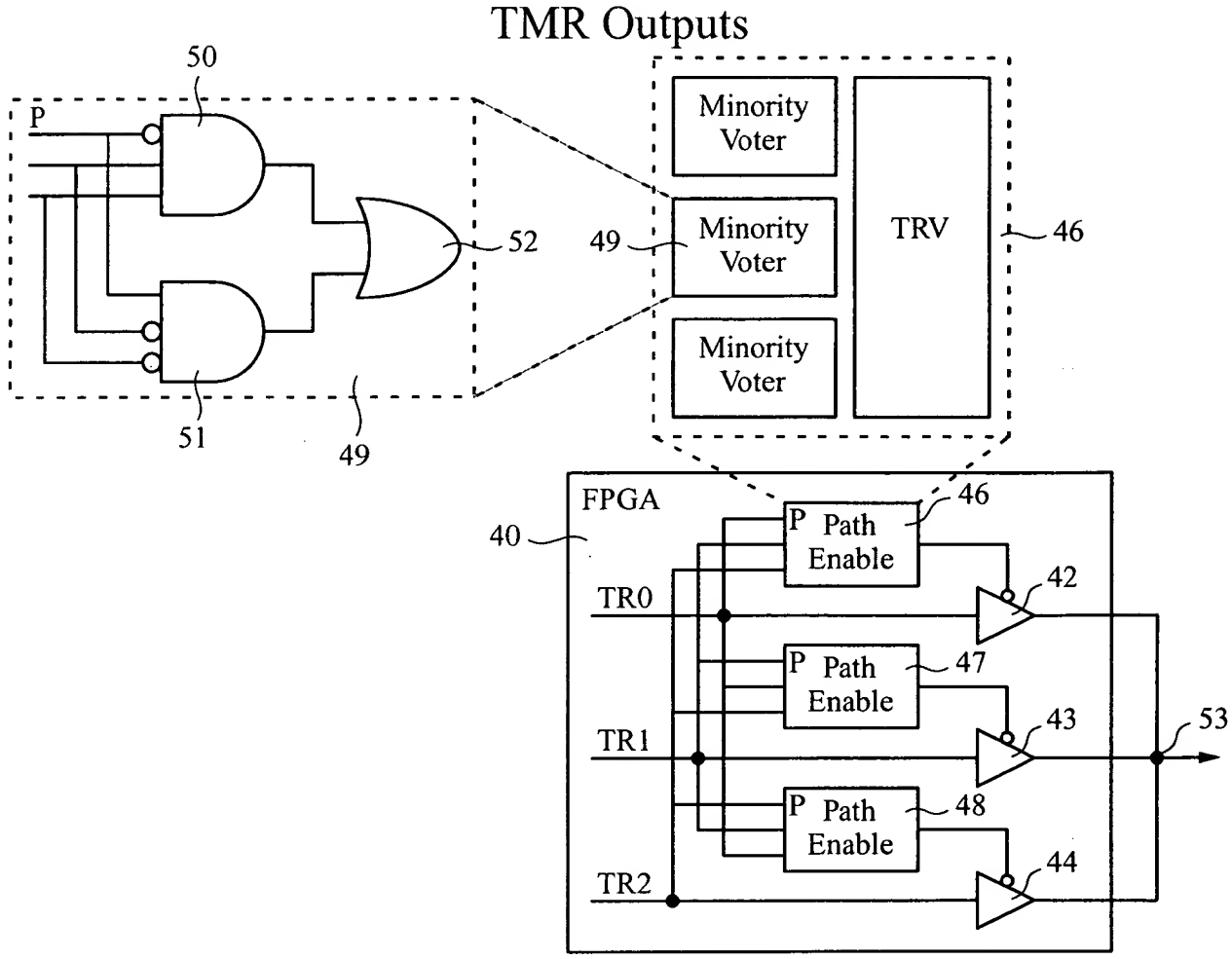
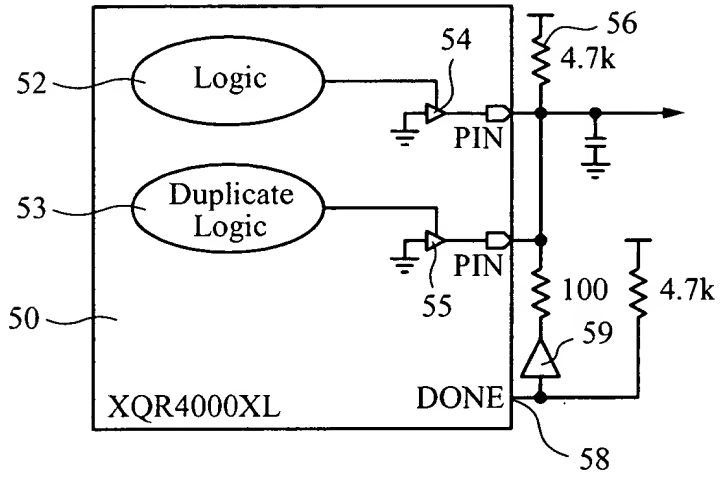
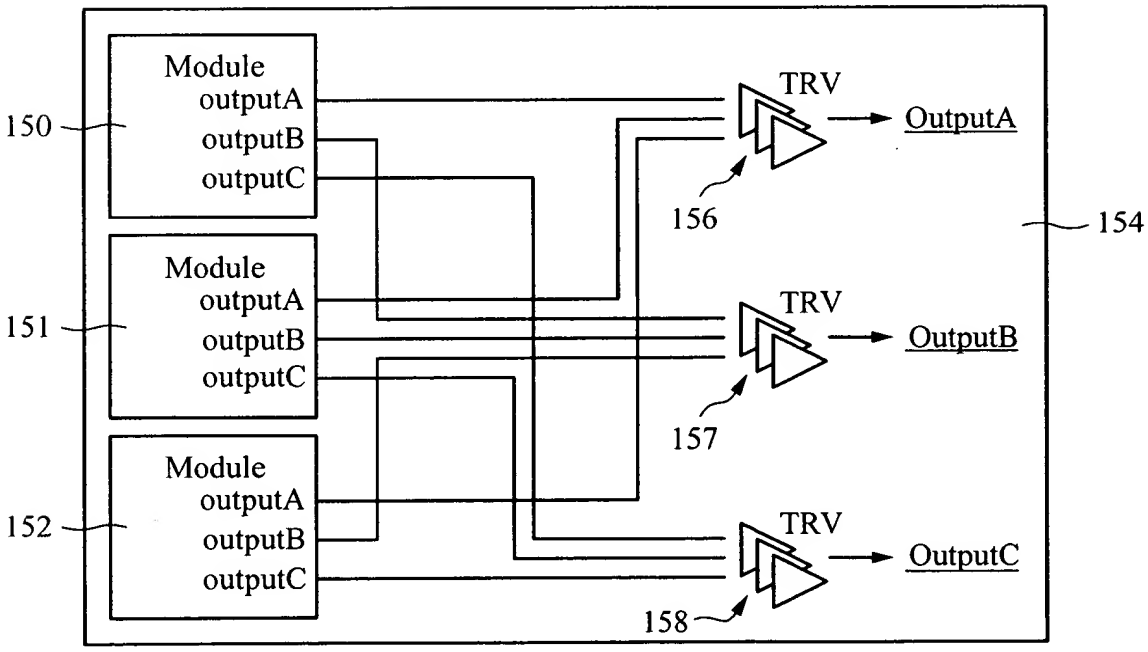

TMR Outputs
50
P
52
51
49
Minority Voter
Minority Voter
Minority Voter
TRV
46
49
FPGA
40
P Path Enable
46
TR0
42
P Path Enable
47
TR1
43
53
P Path Enable
48
TR2
44

FIG. 6



Wire-ANDing Critical Outputs

FIG. 7



Module redundancy and mitigation

FIG. 8

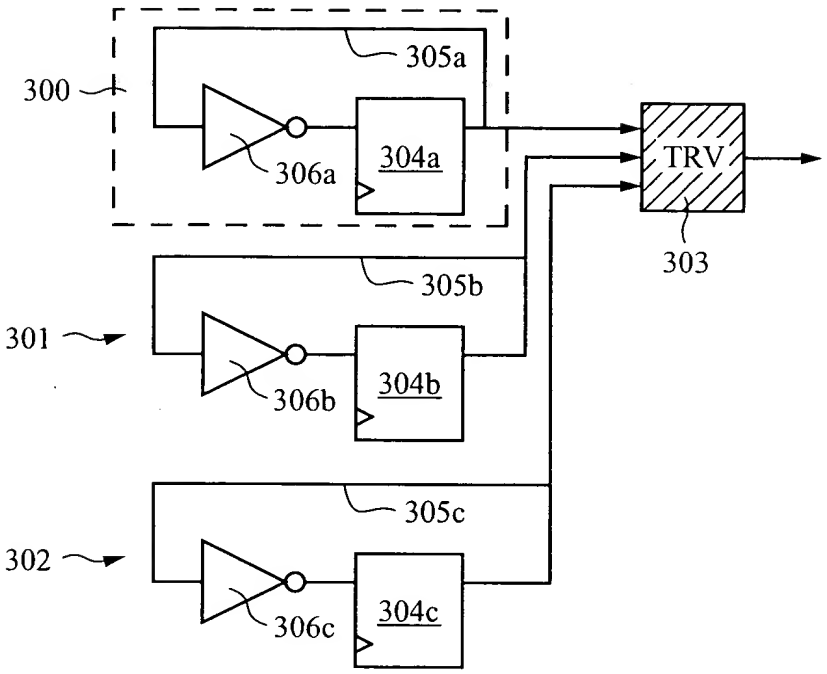

300
305a
306a
304a
TRV
303
305b
301
306b
304b
305c
302
306c
304c

FIG. 9

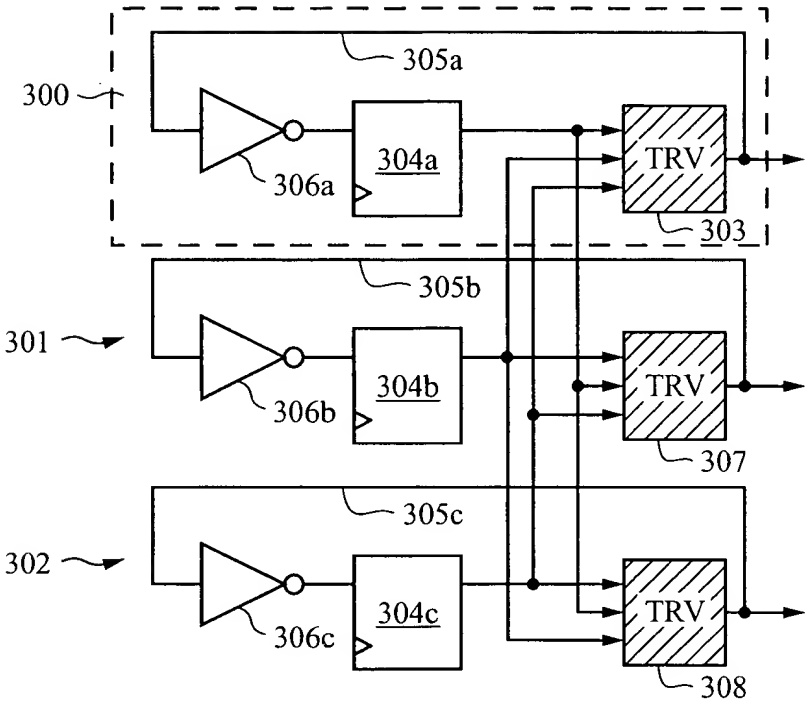
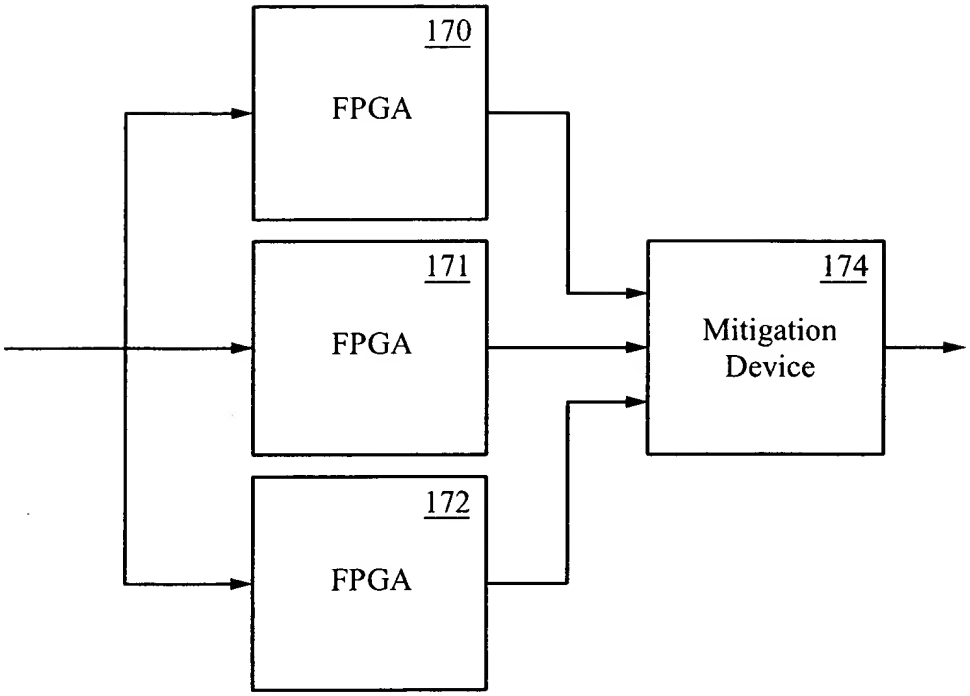
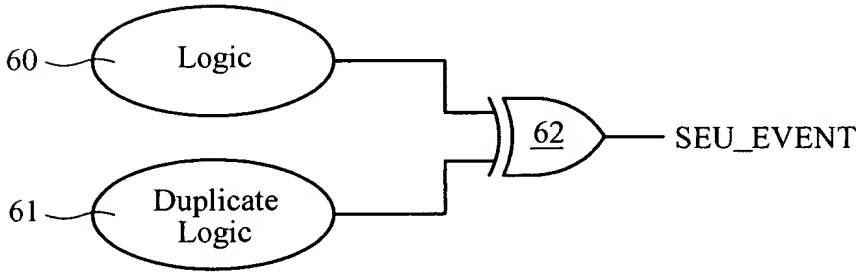

300
305a
304a
306a
TRV
303
301
305b
304b
306b
TRV
307
302
305c
304c
306c
TRV
308

FIG. 10



Triple device redundancy

FIG. 11



SEU Detection by Reundancy and XOR Gating

FIG. 12

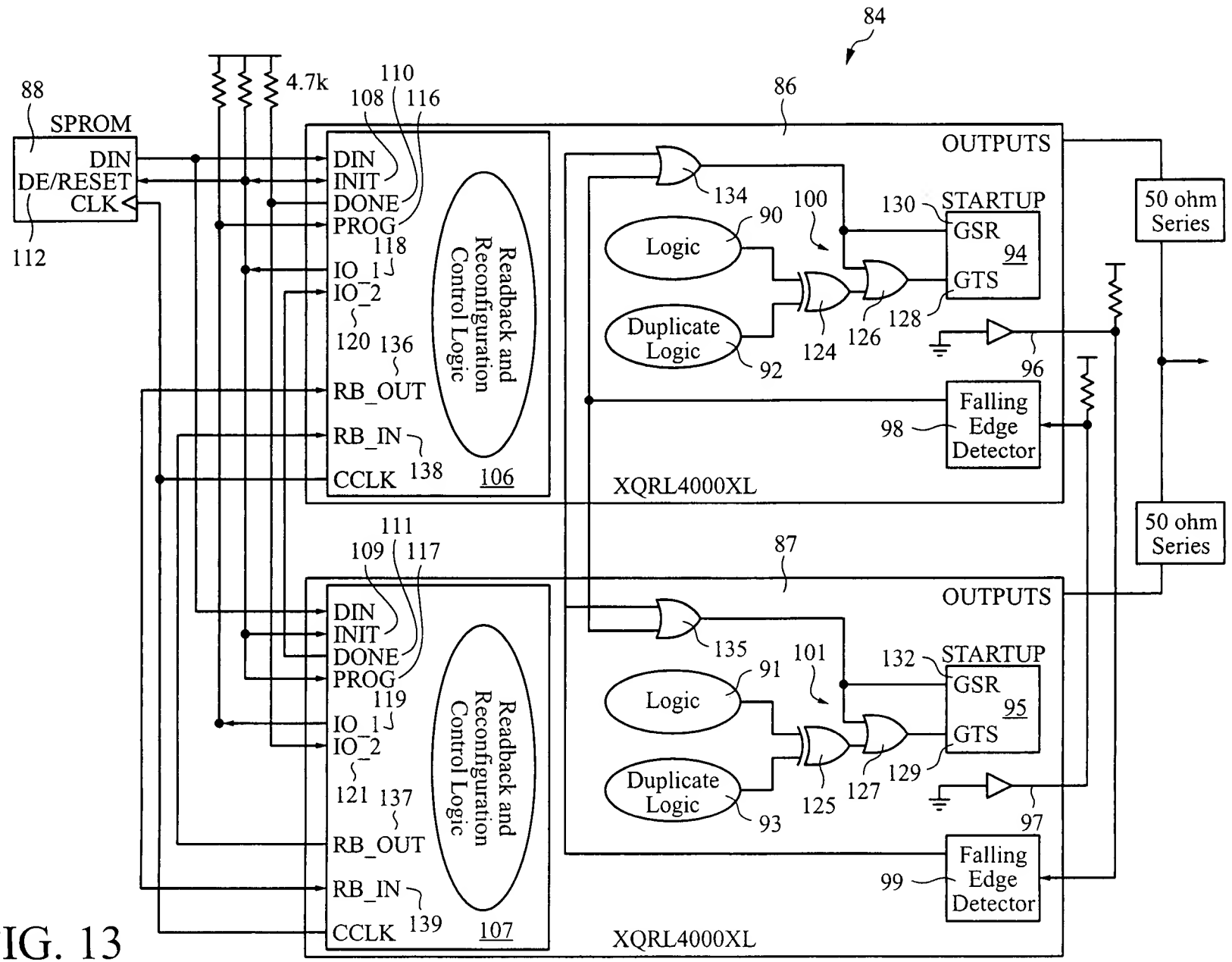

84
88
SPROM
DIN
DE/RESET
CLK
112
4.7k
110
108
116
86
OUTPUTS
DIN
INIT
DONE
PROG
118
IO_1
IO_2
120
136
RB_OUT
RB_IN
CCLK
138
106
Readback and Reconfiguration Control Logic
134
90
100
130
STARTUP
GSR
94
GTS
Logic
Duplicate Logic
92
124
126
128
96
Falling Edge Detector
98
XQRL4000XL
50 ohm Series
50 ohm Series
111
109
117
87
OUTPUTS
DIN
INIT
DONE
PROG
119
IO_1
IO_2
121
137
RB_OUT
RB_IN
CCLK
139
107
Readback and Reconfiguration Control Logic
135
91
101
132
STARTUP
GSR
95
GTS
Logic
Duplicate Logic
93
125
127
129
97
Falling Edge Detector
99
XQRL4000XL

FIG. 13

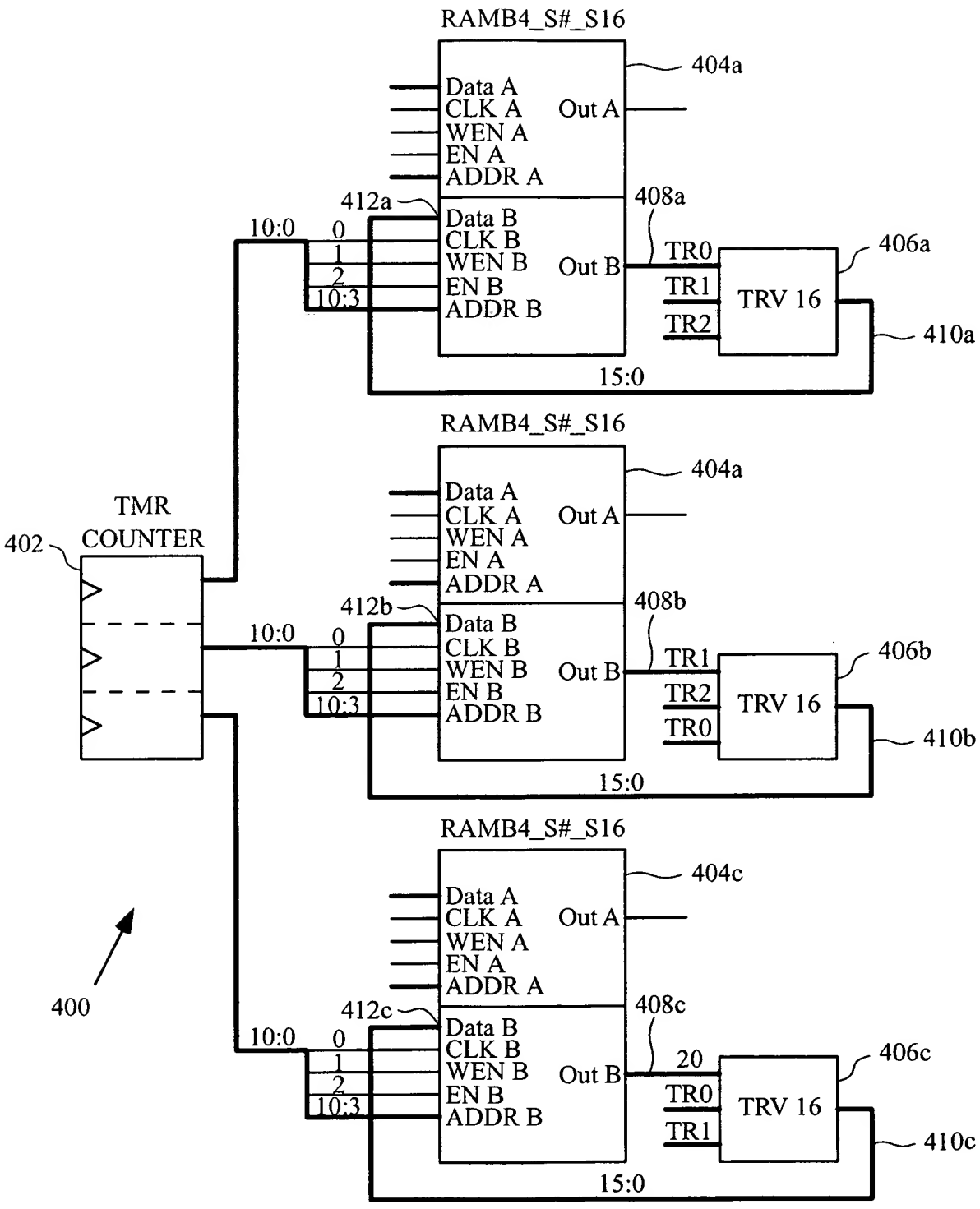

RAMB4_S#_S16
404a
Data A
CLK A
WEN A
EN A
ADDR A
Out A
412a
408a
Data B
CLK B
WEN B
EN B
ADDR B
Out B
10:0
0
1
2
10:3
TR0
TR1
TR2
TRV 16
406a
410a
15:0
RAMB4_S#_S16
404a
TMR
COUNTER
402
412b
408b
406b
410b
RAMB4_S#_S16
404c
412c
408c
406c
410c
20
400

FIG. 14

Patent Pending

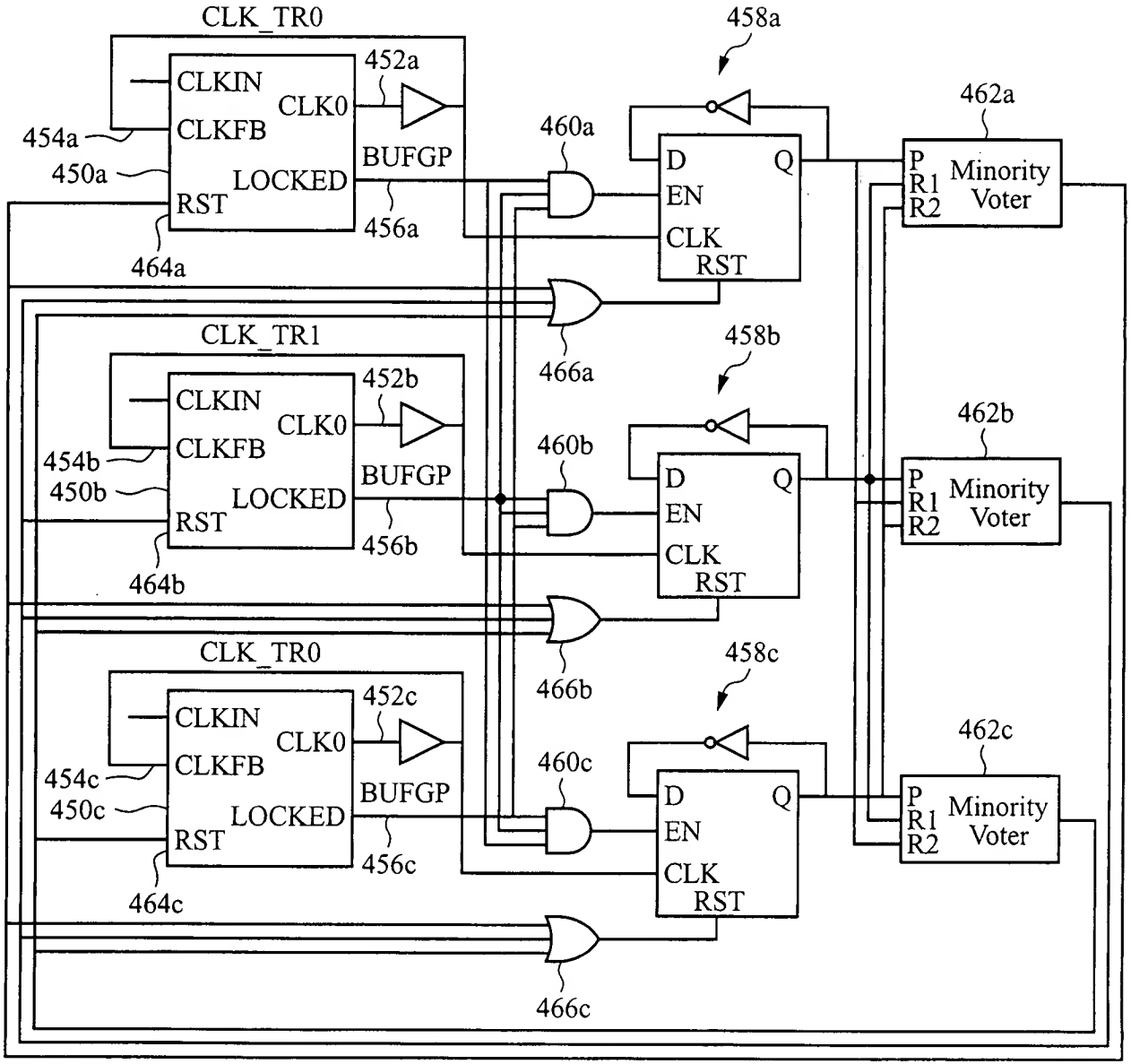


FIG. 15

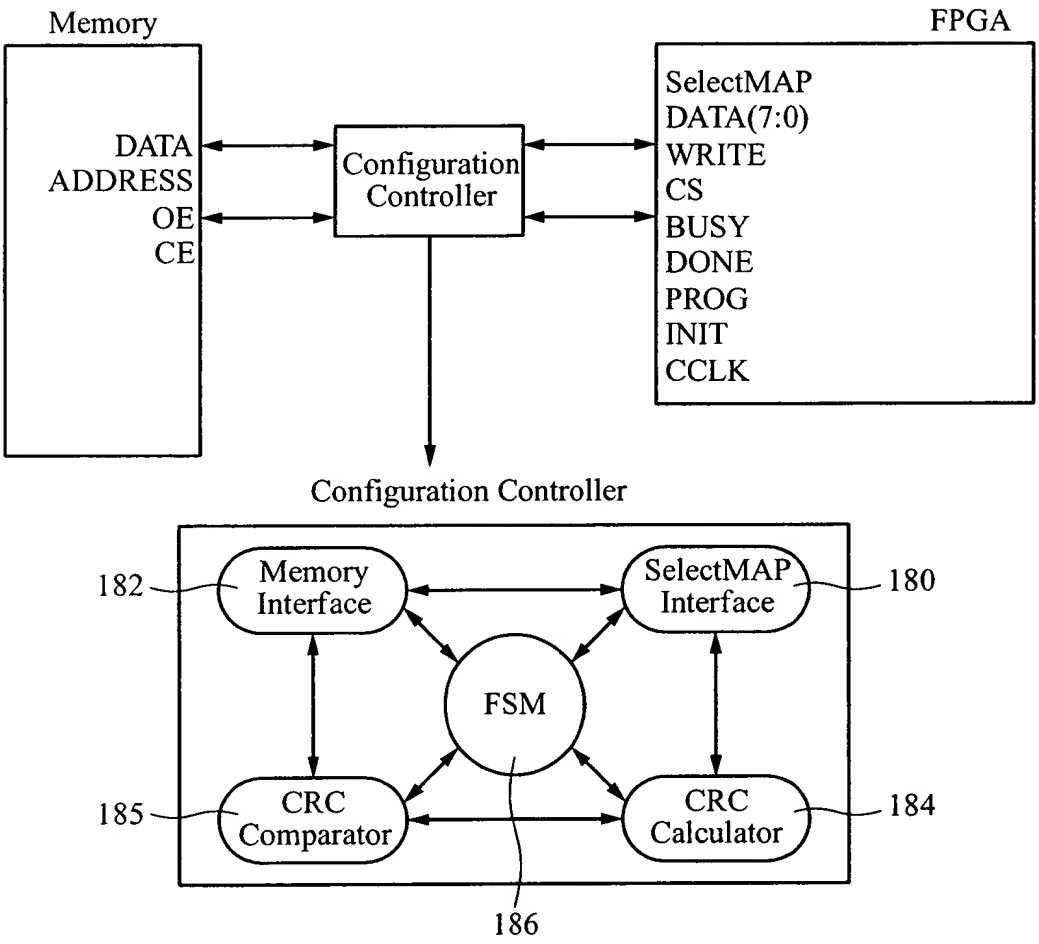
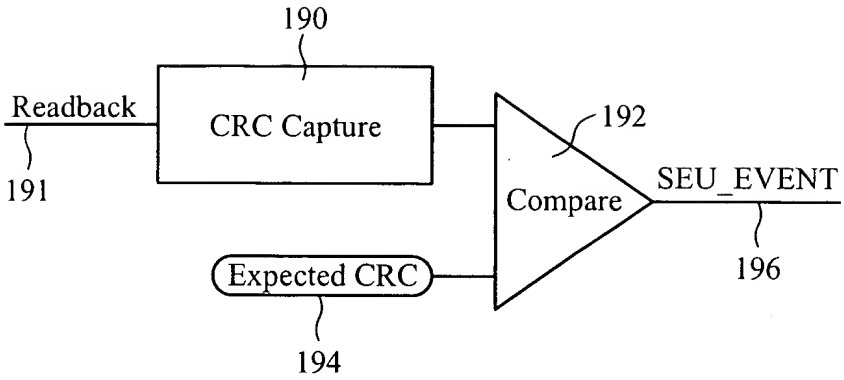
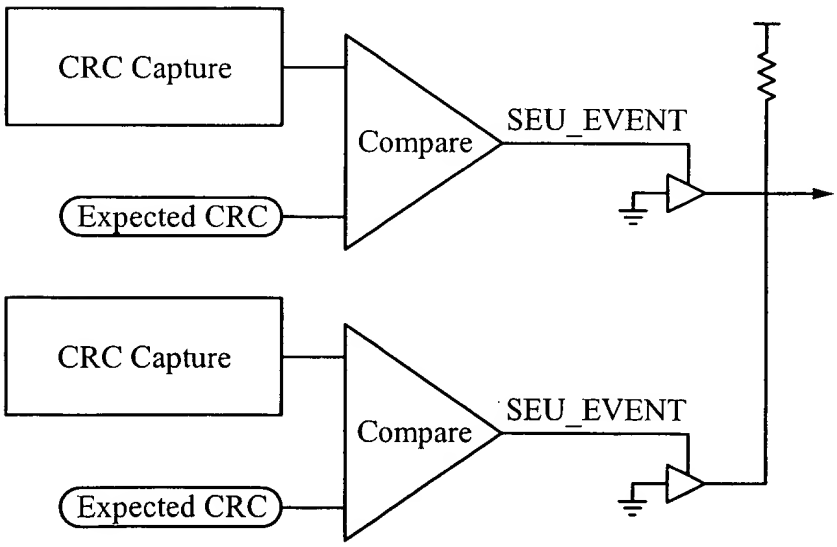

Memory
FPGA
DATA
ADDRESS
OE
CE
Configuration Controller
SelectMAP
DATA(7:0)
WRITE
CS
BUSY
DONE
PROG
INIT
CCLK
Configuration Controller
182
Memory Interface
SelectMAP Interface
180
FSM
185
CRC Comparator
CRC Calculator
184
186

FIG. 16



Readback CRCComparator

FIG. 17



Redundant CRC Comparator

FIG. 18

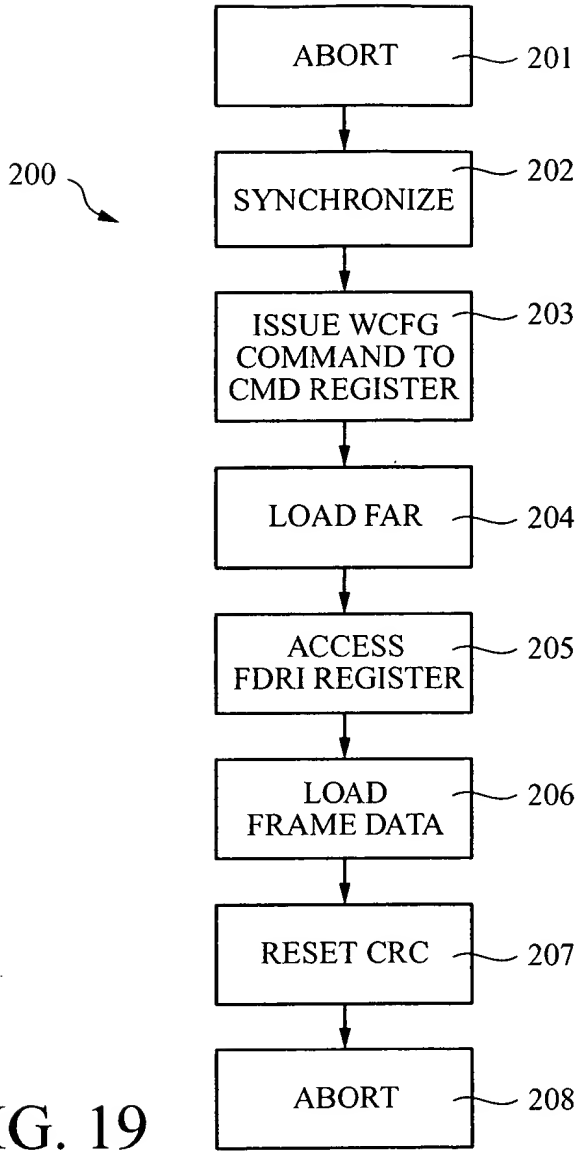
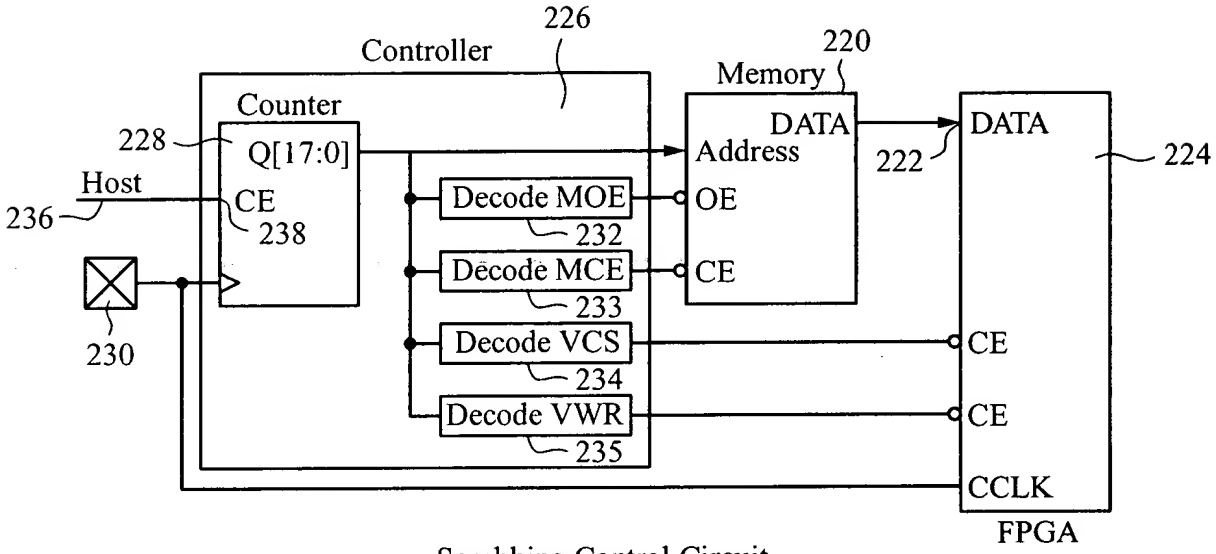


FIG. 19

Instruction Set for Single Frame Write Operation

Command		Data (32 Bits)
Synchronize		AA 99 55 66
Write to CMD		30 00 80 01
WCFG		00 00 00 01
Write FAR		30 00 20 01
Frame Address		0? ?? ?? 00
Write FDRI	XQVR300	30 00 40 2A
	XQVR600	30 00 40 3C
	XQVR1000	30 00 40 4E
Frame Data		
Write CMD		30 00 80 01
RCRC		00 00 00 07

FIG. 20



Scrubbing Control Circuit

FIG. 21

Scrubbing State Transitions

States					Clock Cycles		
Type	MOE	MCE	VCS	VWR	XQVR300	XQVR600	XQVR1000
Load	L	L	L	L	207,972	435,312	745,596
Abort	H	H	L	H	4		
Disable	H	H	H	H	1		

FIG. 22